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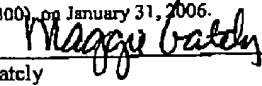
PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

YAMAMOTO et al.Serial No. **10/805,822**Filed: **March 22, 2004**For: **Method of Fabricating Semiconductor
Integrated Circuit**Art Unit: **2815**Examiner: **Wojciechowicz, Edward**Attorney Docket No.: **44471/298721**

CERTIFICATE OF TRANSMISSION UNDER 37 CFR 1.8
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Maggie Gately

Date: January 31, 2006

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The citation of information on the attached Form PTO/SB/08a, "Information Disclosure Statement by Applicant" is made pursuant to 37 C.F.R. §§ 1.56, 1.97, and 1.98. A copy of the non-U.S. patent reference listed is enclosed.

The reference cited on the attached Form PTO/SB/08a was first cited in a Japanese Office Action dated October 25, 2005. A copy of the Japanese Office Action and English translation are enclosed.

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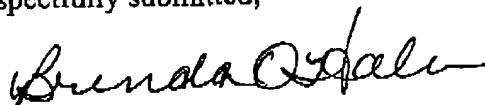
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Appln. No. Serial No. 10/805,822
Page 2 of 2

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As this Supplemental Information Disclosure Statement is being filed after the issuance of an office action on the merits, pursuant to 37 C.F.R. §1.97(c)(2), the fee of \$180, as set forth in §1.17(p), is enclosed. The Commissioner is authorized to charge any additional fees due to Deposit Account No. 11-0855.

Respectfully submitted,



By: Brenda O. Holmes
Reg. No. 40,339

KILPATRICK STOCKTON LLP
1100 Peachtree Street, Suite 2800
Atlanta, Georgia 30309-4530
Telephone: (404) 815-6500
Facsimile: (404) 815-6555
Our Docket: 44471/298721

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Sheet 1 of 1

Complete if Known

Application Number	10/805,822
Filing Date	March 22, 2004
First Named Inventor	Makoto YAMAMOTO et al.
Art Unit	2815
Examiner Name	Wojciechowicz, Edward Joseph
Attorney Docket Number	44471/298721

U.S. PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
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FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ³
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